SUMMARY OF RDS-2000/RDS-3000 DIFFERENCES

IKONAS

1.2 SUMMARY OF RDS-2000/RDS-3000 DIFFERENCES

1.2.1 INTRODUCTION

The RDS-2000 series was produced by IKONAS during 1979-1980. It was built using 10"x10" printed circuit boards, 22 boards per chassis. Each image memory board DR16B contained 64K bytes (512x512x2). In 1981 IKONAS introduced the RDS-3000 which is functionally and programmably almost identical but is produced on a 15"x15" printed circuit board. Each image memory board DR64B contains 256K bytes (512x512x8). This document summarizes differences between the two systems and indicates where software incompatibility may exist.

1.2.2 SYSTEM CAPABILITY

The RDS-3000 provides some enhanced capability over the RDS-2000. The 2000 image memory is limited to 512x512x24 or 1024x1024x8 maximum. The 3000 can be fitted with 1024x1024x24 displayable memory with 2048x2048x32 maximum storage capacity. In addition, the 3000 can have three 8 bit video input channels (RGB digitizer) while the 2000 was limited to a single 8 bit input.

Although there have been and will continue to be new modules with additional capability introduced for the 3000, the basic display memory/graphics processor/matrix multiplier/host computer interface configuration of the 2000 is identical to the 3000.

1.2.3 MODULE DIFFERENCES

Unless otherwise noted here the reader should assume any 2000 software will run on a 3000 system.

1.2.3.1 IMAGE MEMORY

HIRES and LORES pixel addressing are the same for the 2000 and 3000. When displaying in LORES mode a WORD operation in the 2000 affects 2 bits of 16 pixels simultaneously. In the 3000, 4 bits of 8 pixels are affected. When displaying in HIRES mode a word operation in the 2000 affects 1 bit of 32 interlaced pixels; either 32 even pixels or 32 add pixels. In the 3000 1 bit of 32 consecutive pixels is affected. See the DR64B Programming Guide for a full explanation of the 3000 operation.

1.2.3.2 FRAME BUFFER CONTROLLER

Operation is the same for both series except for a slight change in the meaning of pixel dock frequency (Register 5) and X window control during LORES display (Register 2). See the FBC Programming Guide for details.

1.2.3.2.1 CURSOR

The 2000 provided a full screen cross-hair cursor of selectable color. The 3000 provides a 32x32 pixel bit map cursor. Loading of a pattern into the bit map and setting cursor color are explained in the FBC Programming Guide.

1.2.3.3 CROSSBAR SWITCH XBS24

The 3000 crossbar switch has 10 additional bits of overlay and color map page capability. Otherwise the lower 24 bits of the 3000 and 2000 crossbars are identical. See the XBS34 Programming Guide for details.

1.2.3.4 LOOK-UP AND VIDEO OUTPUT

All 3000 systems are built for 10 bit/channel look-up capability. That is, red, green, and blue make up three

10 bit fields as opposed to three 8 bit fields for the 2000 system.

A "channel crossbar switch" was incorporated into the 3000 LUVO version B and later. This channel crossbar allows easy psuedo color control in systems not including the full bit crossbar XBS34. See the LUVO Programming Guide for informaton on its use.

1.2.3.5 BIPOLAR GRAPHICS PROCESSOR

The high performance 32 bit microprogrammable processor is programmed identically for the 2000 and 3000. Full microcode compatibility has been maintained. Debugging on the 3000 has been aided by the incorporation of single step and program counter read-back operation. See the BPS32 Programming Guide for details.

1.2.3.6 MICROCODE MEMORY

In the 2000, the lower 32 bits of 64 bit microcode words are loaded consecutively starting at address 20000$0. The upper 32 bits of microcode words are loaded consecutively starting at address 20100$0. In the 3000 systems, the lower 32 bits are loaded at even addresses and the upper 32 bits at odd addresses beginning with 20000$0.

The IKASM Assembler produces microcode object files which must be loaded in these two different formats. Recent releases of IKASM have incorporated an ORGVEC instruction in the mnemonic file to determine whether the IKASM output is formatted for 2000 or 3000 operation. Check the IKASM manual for details.

The 3000 series microcode memory may be written to by the graphics processor or host computer while the processor is running. This was not possible on the 2000. Thus the 3000 microcode memory may also be used for scratchpad. Again, see the BPS Programming Guide.

1.2.3.7 MATRIX MULTIPLIER

The MA1024 Matrix Multiplier for the 3000 performs the same operations and is microcode compatible with the 2000 unit. The 3000 multiplier optionally allows the input W term to be a stored value rather than always being an implicit "+1" as in the 2000.

1.2.4 SUMMARY

The RDS-3000 has been designed to maintain software compatibility with the RDS-2000 to the greatest extent possible. The changes have been made solely to provide enhanced capability in the 3000 series. Please feel free to contact IKONAS if you have any questions or difficulty when converting from a 2000 to 3000 or vice-versa.