FBC Frame Buffer Controller

General

The FBC is used within the IKONAS RDS-3000 Raster Display System to provide timing and control for the display of images stored in memory. The FBC fetches display data from DR64, DR256, GM64, or GM256 image storage memory and passes this data to a LUVO24/HS color look up table (or optional XBS34 video cross-bar). The FBC provides video sync and format control as well as pan, scroll, and zoom functions and hardware cursor generation.

Display Control

—Lines/Frame 200-2000 (programmable)
—Frames/Sec 20-80 (programmable)
—Interlaced/non-interlaced display (programmable)
—RS-170A/RS-343A sync timing (programmable)
—Pixel Rate 8-45 MHz (programmable)
—Pan/Scroll - Pixel increments
—Memory Size - 512x512 to 2048x2048
—Zoom - integer steps 1, 2, 3, . . . , 16 to 1
—'Lo Res/Hi Res (i.e. select 512x512x24 or 1024x1024x6 display)
—Internal/External Sync (programmable)
—Visible Area (programmable)
—Maximum bits/pixel
—32 LO RES DISPLAY
—24 HI RES DISPLAY
— 32x32 Programmable Cursor

Typical Display Formats

Frame Rate (Hz)	30	30	30	60	60
Lines/Frame	525	551	1103	520	552
Interlace	Yes	Yes	Yes	No	No
Visible Lines	485	511	1023	480	512
Visible Pixels	512-640	512-680	1024-1280	512-640	512
Sync	RS-170A	RS-170A	RS-343A	RS-343A	RS-343A
Notes	1	—	—	2	2

1 — NTSC broadcast standard
2 — Flicker Free

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DR64 Image Memory

General

The DR64 is used within the IKONAS RDS-3000 Raster Display System to store image data for processing and display. The DR64 contains 256K bytes of RAM using 16K memory IC's. Working within the RDS-3000 system the DR64 can receive data from a high speed video input port, supply data to a high speed video display port, and provide random access through a third system port. Multiple DR64's can be used within a system to provide image storage and display of up to 1024x1024 pixels in full color (8 bits each of RED, GREEN, and BLUE).

Storage and Display Capability

—512x512x8 in LO RES MODE 30-60Hz
—1024x1024x2 in HI RES MODE 30Hz
—64Kx32 in WORD MODE-equivalent to eight 4 bit LO RES pixels or thirty-two 1 bit HI RES pixels
—Maximum of twelve DR64 modules per system
  —1024x1024x24 total
  —1Mx32 total

Transfer Rates

—12.0 MByte/sec video input port
—20.0 MByte/sec video output port
—200 NSEC Access, 400 NSEC cycle system port

Compatibility

Fully compatible with all RDS-3000 hardware and software including BPS microprogrammable bit-slice processor, MPC 16 bit microprocessor, and DR256 memory (1MB).

Typical Configurations

Qty. DR64	Storage and Display	Colors
1	512x512x8	256
	1024x1024x2	4
3	512x512x24	16M
	1024x1024x6	64
4	512x512x32	16M+256 overlay
	1024x1024x8	256
12	1024x1024x24	16M

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DR 256 Image Memory

General

The DR256 is used within the IKONAS RDS-3000 Raster Display System to store image data for processing and display. The DR256 contains one megabyte of RAM using 64K memory IC's. Working within the RDS-3000 system the DR256 can receive data from a high speed video input port, supply data to a high speed video display port, and provide random access through a third system port. Multiple DR256's can be used within a system to provide image storage of up to 2048x2048 pixels in full color (8 bits each of RED, GREEN, and BLUE)

Storage Capacity

—1024x1024x8 in LO RES MODE
—2048x2048x2 in HI RES MODE
—256Kx32 in WORD MODE - equivalent to eight 4 bit LO RES pixels or thirty-two 1 bit HI RES pixels
—MAXIMUM of twelve DR256 modules per system
  —2048x2048x24 total
  —4Mx32 total

Display Capability

—1024x512 pixels LO RES 30Hz
—640x480 pixels LO RES 60Hz
—1280x1024 pixels HI RES 30Hz

Transfer Rates

—12.0 Mbyte/sec video input port
—20.0 Mbyte/sec video output port
—200 nsec access, 400 nsec cycle system port

Compatibility

Fully compatible with all RDS-3000 hardware and software including BPS microprogrammable bit slice graphics processor, MPC 16 bit microprocessor, and DR64 memory (256KB).

Typical Configurations

Qty. DR256	Storage	Display	Colors
1	1024x1024x8 2048x2048x2	512x512x8 1024x1024x2	256 4
3	1024x1024x24 2048x2048x6	512x512x24 1024x1024x6	16M 64
4	1024x1024x32 2048x2048x8	512x512x32 1024x1024x8	16M+256 overlay 256
12	2048x2048x24 2048x2048x24	512x512x24 1024x1024x24	16M 16M

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LUVO24/HS Video Look-Up and Output

General

The LUVO24/HS is used within the IKONAS RDS-3000 Raster Display System to provide translation from stored image value to displayed color. Over 16 million colors can be displayed. The LUVO24/HS receives image data from an FBC Frame Buffer Controller (or optional XBS34 Cross Bar Switch), selects full color or pseudo-color data, determines displayed values by addressing color look-up tables, and provides video output to drive a color monitor.

Organization

Image data (up to 24 bits/pixel) is supplied to the LUVO24/HS and feeds three independent channel selector circuits (RED, GREEN, and BLUE CHANNELS). Each circuit programmably selects 8 bits of the input pixel data to address a color look-up table. Two additional address bits are provided by the FBC Frame Buffer Controller (cursor and page select). Three ultra high speed video digital-to-analog converters are supplied 8 bit (256 level) values from the color maps. Standard video outputs can then be connected to a color display monitor.

Display Capability

- —5-45MHz pixel rate
- —512x512 (30Hz), 512x512 (60Hz), 1024x1024 (30Hz) display rates
- —16 million colors

Channel Selector

- —Three 8 bit channel inputs
- —Three 8 bit channel outputs (RED, GREEN, BLUE)
- —Any output channel can be connected to any input channel under software control for full color or pseudo-color operation

Color Look-Up Tables

- —Three 1024x8 tables (RED, GREEN, BLUE)
- —Table input
  - —8 bits from channel selector for data display
  - —1 bit from hardware cursor (32x32 pixels) for solid, reverse, bright cursor effects.
  - —1 bit from control register for software alternate map selection
- —Tables Read/Written from IKONAS system bus by host computer, graphics processor, or peripheral microprocessor

Digital-To-Analog Converters

- —Three 8 bit low-glitch video DAC (256 levels)
- —Ultra-high-speed (10 nsec settling time)
- —75 ohm 1 volt output
- —Non-composite video output (composite optional)

Options

- —LUVO30/HS
  - —1024x10 look up tables
  - —10 bit DACs (1024 levels)
  - —15nsec settling time
  - —Useful in critical video applications
- —Overlay
  - —Allows overlay data to supercede normal display
  - —8 additional input bits to LUVO24/HS
  - —Up to 256 overlay colors displayed
  - —Overlay colors use alternate map values
  - —Normally requires XBS34 option
- —XBS34
  - —See separate spec for full details
  - —Allows 10 bit pseudo-color (1024 colors)
  - —Arbitrary RGB bit assignment

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XBS34 Video Cross Bar Switch

General

The XBS is an option used within the IKONAS RDS-3000 Raster Display System to provide maximum flexibility in image display. The XBS allows a user to programmably select bits of stored image pixels to be used for display. The XBS34 receives image data from the FBC Frame Buffer Controller and passes data to the LUVO24/HS Look-Up and Video Output Module for display. Each bit of output can be programmably selected to come from any bit of input allowing maximum flexibility for high-performance applications.

Input

Input to the XBS34 consists of 35 bits per pixel. Thirty-two bits are supplied by image memory scanned out under control of the FBC. Two bits are set by a control register within the FBC. One bit is supplied from the FBC hardware cursor circuit (a 32x32 bit pattern).

Selection

The XBS34 contains 34 control registers. Each control register corresponds to a particular output pixel bit and can be written via the IKONAS BUS by host computer, graphics processor, or peripheral microprocessor. Each control register's contents selects one of 35 input bits, or a constant zero, for output.

Output

The XBS34 output connects to the LUVO24/HS Look-Up and Video Output Module. Twenty-four output bits supply normal display data. Eight bits supply overlay data (for LUVO overlay option). Two bits supply color look-up table high address (page) bits.

Summary

- —Input
  - —32 image data bits
  - — 2 register bits
  - — 1 cursor bit
- —Selector
  - —34 control registers
- —Output
  - —24 image data bits
  - — 8 optional overlay bits
  - — 2 look-up table page bits

Uses

The XBS34 allows maximum flexibility in multi-band image processing situations. It is also extremely useful for double-buffering or other graphics animation applications.

/Fill Option

The /Fill option contains hardware to allow an output bit to remain ON from one occurence of an input pixel bit to the next. Thus a pair of vertical lines in image memory would create a filled rectangle display. This option is useful for applications requiring large filled areas such as mapping, IC layout, and solid modeling. Only 24 image data input bits can be used with the /FILL option. Eight of these feed separate fill circuits and are then available to the selector circuits as image data inputs 24-31. All other XBS34 functions remain unchanged.

- —8 independent filled bit planes
- —256 fill colors possible
- —video rate fill

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GPS Graphics Processor Set

General

The Graphics Processor Set is used within the IKONAS RDS-3000 Raster Display System to provide high-speed high-performance graphics generation and image processing capability. The GPS consists of the following items:

—BPS - 32 bit microprogrammable bit-slice processor
—MCM4 - 4Kx64 microcode RAM
—SR8 - 8Kx32 high speed scratchpad RAM
—IKASM-microcode cross assembler software

The Graphics Processor is connected to the RDS-3000 IKONAS BUS, a high-speed 32 bit system bus providing full access to all elements within the system. The Graphics Processor can create graphics for display, manipulate existing images, create color look-up tables, and control system registers (pan, scroll, zoom, cursor, etc.) A user may operate with standard microcode supplied by IKONAS or program special functions for maximum capability when needed.

Performance

The Graphics Processor Set performance can best be evaluated by looking at timing for typical graphics generation tasks within the IKONAS RDS-3000 system.

Vectors
—4-6 microsec set-up
2 million pixels/sec drawing rate
Polygons
—4-6 microsec set-up per vertex
1 million pixels/sec drawing rate
Rectangles (WORD MODE)
—4 microsec set-up
32 million pixels/sec drawing rate

Add two 512x512x8 images - 0.3 seconds
Load Ramp to Color Map - 110 microsec.
Raster Op (move rectangular array of pixels)
—4 microsec set-up
—1 million pixels/sec move

IKASM

IKASM is a microcode cross assembler written in FORTRAN for installation on the user's host computer. Input to IKASM consists of microcode text files and mnemonic definition files. IKASM produces microcode object files capable of being down-loaded by the general purpose file loader IKLOD. Once microprograms are down-loaded to the MCM4 they can be executed by the BPS. IKASM is used for assembling IKONAS supplied microprograms as well as any user developed microcode.

BPS

The BPS bit-slice processor is a 32 bit wide device with a 200 nsec cycletime. The BPS contains sixteen internal 32 bit registers, a 32 bit ALU, a 16x16 hardware multiplier, and a microprogram controller. It executes 64 bit instructions stored in the companion MCM4 memory. The 32 bit ALU can be operated as two parallel 16 bit sections for a doubling of performance in critical applications. The 64 bit wide instruction and BPS architecture allow several operations to be executed concurrently. For example in one instruction the BPS can simultaneously:

1) ADD two 32 bit registers
2) SHIFT the result and store into another register
3) MULTIPLY two 16 bit numbers
4) WRITE data to a pixel for display
5) INCREMENT a loop counter
6) BRANCH to a subroutine conditionally

All within 200 nsec.

MCM4

The MCM4 microcode RAM stores the microprograms to be executed by the BPS. This 4Kx64 memory is implemented with 55 nsec dual ported RAM with an IKONAS BUS port for writing/reading microcode and a 64 bit port for microcode execution. The MCM4 can be used by the BPS for general purpose storage when necessary. Additional MCM4 boards may be added to the RDS-3000 for extraordinarily complex applications.

SR8

The SR8 scratchpad RAM is used by the BPS microprogram for general purpose high speed storage. Vector lists, command strings, etc. are stored in this memory for use by microprograms. This 8kx32 memory is implemented with 55 nsec dual ported RAM. One port is connected to the IKONAS BUS for read/write access and the other is available for an auxillary hardware processor such as the MA1024 Matrix Multiplier. Additional SR8 boards may be added to the RDS-3000 for increased high-speed storage. For very large storage applications the DR64 (64Kx32) or DR256 (256Kx32) memories can be used with a 200 nsec increase in access time.

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IDL IKONAS Display Language

General

The IDL software package enables a user to write display programs which will be executed by the Graphics Processor within an IKONAS RDS-3000 Raster Display System. The package consists of an IDL COMPILER (written in FORTRAN) and IDL DISPLAY MICROPROGRAMS (written in IKASM). The COMPILER is installed on the customer's host computer and used to produce IDL OBJECT FILES. IDL OBJECT FILES are down-loaded to the IKONAS RDS-3000 to control execution of previously down-loaded DISPLAY MICROPROGRAMS. A SYMBOL TABLE is also produced by the IDL COMPILER so that run-time modification of data or commands by host computer programs is possible.

IKONAS Display Language (IDL)

IDL allows easy programming of stand-alone graphics display programs. IDL commands define display lists, manipulate display lists, control display, and control program flow. For example, a simple IDL program might:

(1) define AIRCRAFT-LIST
(2) define RUNWAY-LIST
(3) read 3-D joystick
(4) construct AIRCRAFT-TRANSFORM
(5) construct RUNWAY-TRANSFORM
(6) transform AIRCRAFT-LIST
(7) display AIRCRAFT-LIST
(8) transform RUNWAY-LIST
(9) display RUNWAY
(10) display "FOUR MILES TO TOUCHDOWN"
(11) read function switches
(12) branch to (3) or halt

IDL Commands

There are 128 IDL command codes reserved for IKONAS use and 128 available for user written and defined codes. Some of the standard commands are:

- —Display Vector List
  - —Dashed/Solid
  - —Absolute/Relative
- —Transform Vector List
- —Clip Vector List
- —Display Character String
- —Display Circles, Rectangles
- —Display Filled Areas
- —Create Transform
- —Create Vector List - MOVE/DRAW
- —Program Loop
- —Move Data
- —Program Branch
- —CONSULT IDL MANUAL FOR FULL LISTING—

IDL Compiler

- —Written in FORTRAN
- —Input: IDL-TEXT FILE
- —Output:
  - —IDL-OBJECT FILE (commands and data)
  - —IDL-LISTING FILE (program listing)
  - —IDL-SYMBOL FILE (pointers to data)

IDL Microprograms

- —Microcode source text supplied
- —Assembled with IKASM cross-assembler
- —Version for HI RES, LO RES display
- —Versions for
  - —hardware transforms
  - —hardware characters
- —User Routines can be added

USES

IDL is most useful when pre-defined display formats are needed (command/control, cockpit display, simulation, CAD/CAM, etc.). The IDL DISPLAY MICROPROGRAMS can also be used to develop support for other graphics packages.

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MPC Peripheral Controller

General

The MPC is used within the IKONAS RDS-3000 Raster Display System to provide an interface to multiple interactive devices under local microprocessor control. The MPC is a powerful building block for workstation and standalone configurations since it incorporates a Motorola 68000 16-bit microprocessor with up to 512K bytes of memory. The current software release consists of a multi-tasking real-time monitor with interactive control routines. Provision is also made for user-written programs to run under the monitor. Ikonas plans to release the UNIX (TM-WESTERN ELECTRIC) System for the MPC during 1982 with memory mapping and Winchester disk unit.

Features

—68000 microprocessor with 32 bit internal data, 16 bit external data, 24 bit address, 8MHz.
—4 serial ports, 1 parallel port (16 bits I/O)
—Bus extension port (16 bits data, 24 bits address)
—Direct IKONAS BUS access to entire 68000 address-space (program, data, peripherals, etc.)
—Mapped 68000 access to entire IKONAS BUS address space (control registers, image memory, color map, etc.)
—32KB RAM, 8KB ROM
—Interactive device monitor software

Options

—512KB RAM
—Peripheral Expansion Unit
—Interactive Devices

PCP Peripheral Expansion Unit (optional)

—Connects to parallel port on MPC
—4 additional serial ports
—8 parallel ports (16 bits I/O)
—16 Analog ports (+/-10V, 12 bit digitization)
—Rack mounted unit

Interactive Devices (optional)

—DT11 - Data Tablet (11"x11") - serial
—TB3 - Track Ball (3") - serial
—CRTI - CRT Terminal - serial
—BB16 - Sixteen Lighted Switches - parallel
—DB8 - Eight Control Dials - analog
—JS3 - Three Axis Joystick - analog

Software

—Support routines for all interactive devices
—Pan, scroll, zoom, viewport, cursor control
—Multi-tasking monitor including user interface and debugging aid
—68000 cross-assembler for DEC PDP-11, IBM 370, and time-sharing service available from Motorola for user program development.

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MA1024/D Matrix Multiplier

General

The MA1024/D is used within the IKONAS RDS-3000 Raster Display System for 2-D and 3-D transformations of items to be displayed. It can be used for displays involving vectors, polygons, curved surfaces, and solids. Data used by the MA1024/D must be stored in one or more SR8 high speed memories. A special bus connects the MA1024/D with the SR8(s) to maximize throughput. In typical use a vector list is loaded into an SR8 by the system's host computer. The MA1024/D fetches and transforms the list and the result is used by the BPS graphics processor for display. The MA1024/D can store sixty-four 4x4 transformation matrices for sophisticated data manipulation and is user microprogrammable for specialized applications.

Operation

The MA1024/D fetches data from an attached SR8 memory, multiplies this data by coefficients stored internally, accumulates results, and writes these back to the attached SR8 for use by the Graphics Processor. This process is controlled by an internal microprogram started upon command from the Graphics Processor. User written microcode can be executed for special applications such as B-spline surface evaluation, normal calculations, etc. Control registers determine function performed and data to be used.

Operational Features

- —1Kx16 Matrix Coefficient RAM
- —16x16 bit multiply
- —35 bit accumulate
- —16 bit input X, Y, Z, W
- —16 bit output X, Y, Z, W (transformed)
- —12 bit output X, Y, Z (w/perspective division)
- —Six comparators aid 3-D clipping
- —Operation transparent to system

Control Features

- —Input list Address Register
- —Output list Address Register
- —List Counter Register
- —1Kx32 microprogram RAM
- —Function register
  - —2-D transform (833,000 points/sec)
  - —3-D transform (417,000 points/sec)
  - —3-D transform with perspective (278,000 points/sec)
  - —User written functions (5 million operations/sec)

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VI8 Video Input Digitizer

General

The VI8 is used within the IKONAS RDS-3000 Raster Display System to provide real-time digitization and storage of video input from a television camera or video tape recorder. The VI8 allows programmable control of area to be digitized, image storage location, and other variables for maximum flexibility. Video input is digitized to eight bit accuracy after analog processing.

Digitizer

—75 ohm input 1 volt nominal
—Adjustable analog gain and offset allow digitization of small signal variations
—8-13 MHz sampling rate (programmable)
—External sample clock input
—8 bit/sample digitization
—External sync input
—Composite, vertical, horizontal sync outputs
—525 line, 30 frames/sec typical

Storage Control

—Single-frame mode (1/30 second)
—Continuous mode
—Programmable digitized area 16x16 to 512x512
—Programmable minification 1:1 to 16:1
—Image digitized from programmable video location
—Image stored at programmable memory location
—Sequential images can be stored (at 30 frames per second) to different locations
—Write mask allows 1-8 bit storage

Option

—VI24 - Three eight bit digitizers for real time RGB input and storage

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IF/IK Host Computer Interface

General

The IF/IK is a general purpose host computer interface for the IKONAS RDS-3000 Raster Display System. An interface unit for a specific host computer connects to the IF/IK. Interface units for most popular mini-computers are available. The IF/IK allows the host computer to access all image memory, control registers, data memory, etc. within the RDS-3000 system. The host computer can read and write data in programmed input/output (PIO) or direct memory access (DMA) modes.

Features

- —PIO or DMA transfers (programmable)
- —6.7 megabyte/sec maximum transfer rate
- —Auto increment addressing
- —X, Y addressing of image memory
- —Auto 8 bit to 16 bit pack/unpack
- —Auto 16 bit to 32 bit pack/unpack
- —Three host control registers, four IKONAS control registers ensure easy software portability
- —Host computer has direct read/write access to all RDS-3000 features
- —Two 50 conductor cables connect IF/IK to host

Host Computer Interface Units

- —IK11B
  - —DEC PDP-11, VAX UNIBUS (16 bit)
- —IKQ
  - —DEC LSI-11 Q-BUS (16 bit)
- —IF/NOVA
  - —Data General Nova, Eclipse (16 bit)
- —IF/SEL
  - —Gould/Sel HSD (32 bit)
- —IF/PR
  - —PRIME GPIB (16 bit)
- —IF/PE
  - —Perkin/Elmer 02-304 ULI (16 bit)
- —IF/ROLM
  - —ROLM 3564 (16 bit)

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RK5 and RK6 Equipment Racks

Equipment Racks RK5 and RK6 are designed to house IKONAS RDS-3000 display systems as well as providing standard 19" rack mounting space for other computer and video equipment. Cooling fans and ventilation grilles are included.

Overall Size:

RK5 - 60" high x 30.75" deep x 21" wide
RK6 - 86" high x 30.75" deep x 21" wide

Usable Mounting Area:

RK5 - 45.5" high x 29.5" deep
RK6 - 71.75" high x 29.5" deep

Equipment Dimensions:

IKONAS CB12 - 22.75" high x 27" deep
IKONAS PCP - 17.5" high x 6" deep
Tektronix 1474 Sync Gen - 3.5" high x 17" deep
Fernseh TCE 3000 NTSC Encoder - 1.75" high x 17" deep

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IDSS IKONAS Display Support Subroutines

General

The IKONAS DISPLAY SUPPORT SUBROUTINES (IDSS) are a set of FORTRAN subroutines for communication with the IKONAS RDS-3000 Raster Display System. IDSS subroutines reside in the host computer and provide support for high-level Core-like display and image management routines, without sacrificing IKONAS flexibility and performance.

IDSS subroutines free the user from concern about physical addresses, control registers, write masks, etc. A single call will write to an IKONAS device; the user can provide all the necessary data or rely on standard defaults. The subroutines facilitate such operations as general-purpose image loading and multiple buffering (ping-pong). A MOVIELOOP subroutine provides easy-to-use, flexible animation capabilities.

IDSS Features

--define an area of memory for display
--set display characteristics
--load the color maps
--select color map input
--update image memory
--define the cursor
--read back values previously written to image memory and to IKONAS registers
--write to other IKONAS devices

Updating Image Memory

A single call can fill a user-defined area of memory from a pixel data array. Routines are available to write/read rows or blocks of pixel data, word, halfword, or byte data.

IDSS simplifies addressing the frame buffer by allowing users to define subsets of image memory called logical frame buffers. These can be further subdivided into viewports. Each viewport has its own virtual address system, eliminating the need to calculate physical addresses. All updates affect the current viewport; and when a logical frame buffer moves, it takes all its viewports with it.

Defining the Display

IDSS subroutines aid the user in defining a display frame buffer, which determines the area of memory to be displayed on the screen.

Other subroutines define characteristics of the raster scan (frame rate, lines per frame, sync type, interlace, pixel clock). Alternatively, an initialization routine will set these registers according to a table of default values.

Loading the Color Maps

The color maps contain look-up tables to convert pixel input data into intensities of red, green and blue for the video output. IDSS subroutines load the color maps with a user-defined array, a gamma function, or a ramp (user specifies only the first and last value in the ramp). The channel crossbar can be used to select full color or pseudo-color.

Setting the Crossbar Switch

The video crossbar switch selects bitplanes for input to the color maps. Routines are available to set identity or a particular configuration.

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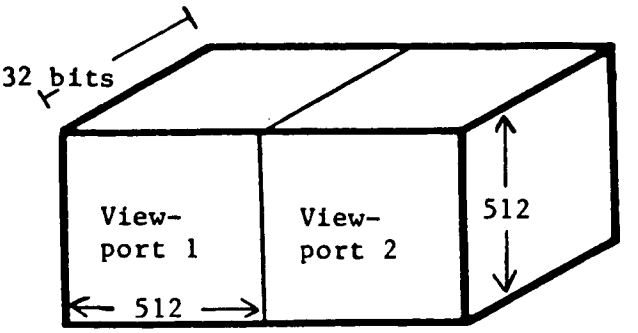
Double-Buffered Display



Example
Logical Frame Buffer - 1024x512x32, LORES
Two Viewports, each 512x512x32
Display Frame Buffer - 512x512x32, LORES

o User program:

  Call KDLFB to define logical
  frame buffer by size
  (in pixels), depth (in bits),
  resolution
  Call KDVPT to define each viewport
  by size, location, bitmask
  Call KDDFB to define display
  frame buffer by size,
  bitmask, resolution
  Program loop:
  Call KSVPT(1) to set
  viewport #1
  User program updates viewport #1
  Call KMDFB(X1, Y1...) to position display frame buffer
  Call KSVPT(2) to set viewport #2
  User program updates viewport #2
  Call KMDFB(X2, Y2...) to move display frame buffer

o Viewport update addresses are pixel addresses from (0,0) to maximum specified in viewport definition.

o Another means of double-buffering is to define viewports with the same x,y location but with different bitmasks.

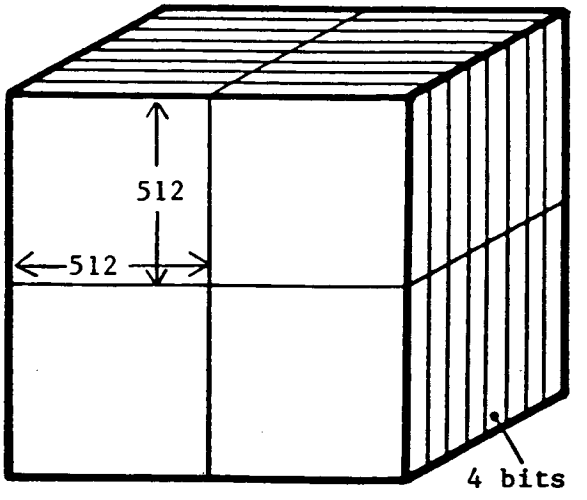
Movieloop or Colormap Animation

o Write pixel data to image memory

o Define data list giving
  -location of each frame in x,y,
  channel(s), bitplane(s),
  colormap/frame...
  -attributes (zoom, screensize...)

o Call MOVIELOOP with datalist
  name, number of frames, rate
  of display, loop execution
  type (once through and quit,
  reverse loop, etc.)...

o Optionally, the MOVIELOOP
  routine can call a user
  subroutine to change parameters
  dynamically. For example, a
  user subroutine could read data
  from a peripheral device such
  as a JOYSTICK or BUTTON BOX to
  change the display rate, data
  list attributes, etc.



Example
32 frames - each frame is
512x512x4, LORES

APEX
Graphics Generator

PRODUCT ANNOUNCEMENT - SIGGRAPH '82

APEX High Speed Graphics Generator

The APEX Graphics Generator is used within the IKONAS RDS-3000 Raster Display System to provide very high performance graphics generation ideally suited to cost-effective advanced work station configurations.

The APEX, working in conjunction with GM64 or GM256 image memories, can write up to 64 million pixels/second maximum. For typical tasks such as polygon fill for solid modeling, an average of 32 million pixels/second can be filled.

In addition, the microprogrammed bit slice processor used in the APEX can perform character generation at 32 million pixels/second typical and vector generation at 2 million pixels/second. Additional functions will be added to the APEX shortly.

Although not as flexible as the Ikonas GPS Graphics Processor, the APEX offers remarkable speed improvement in critical areas at less than a third the price. Available in the fourth quarter of 1982.

NEW PRODUCT

IKONAS