OUTSTANDING FEATURES OF THE IKONAS RDS-3000 PRODUCT LINE

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1. PROGRAMMABLE DISPLAY FORMATS

In RDS-3000 systems, the line rate, frame rate, and pixel clock rate are all user programmable. This allows multiple display formats to be output from a single display system. Possible formats include:

Using the DR64B Image Memory

1. 512 x 512 30 Hz interlaced refresh; 4 to 3 or 1 to 1 aspect ratio
2. 512 x 512 60 Hz non-interlaced refresh; 4 to 3 or 1 to 1 aspect ratio
3. 512 x 480 30 Hz interlaced refresh, NTSC Compatible
4. 1024 x 1024 30 Hz interlaced refresh; 4 to 3 or 1 to 1 aspect ratio

Using the DR 256 Image Memory

5. 640 x 480 30 Hz interlaced refresh, NTSC Compatible
6. 1280 x 960 30 Hz interlaced refresh

2. LARGE IMAGE MEMORY

Using the DR64B Image Memory, the maximum stored and displayed image is 1024 x 1024 x 24 bits.

Using the DR256 Image Memory, the maximum stored display is 2048 x 2048 x 24 bits of which up to 1280 x 1024 may be viewed at any one time.

Image Memory may be added to the system as a field upgrade. No backplane rewiring is required.

3. FULLY USER PROGRAMMABLE DISPLAY PROCESSOR

The 32 bit, 200 nsec Display processor is fully user programmable. There is basic set of graphics software microcode available from IKONAS, but the user is able to develop his own specific applications code. The Processor is highly parallel in operation with a 64 bit microcode word.

As an example of the amount of parallelism achieved, the processor can add two registers and store the result in a

third, multiply two 16 bit numbers, write a previously computed value to image memory, and conditionally call one of two subroutines all in a single cycle.

The processor includes a hardware multiplier chip which allows a 16 x 16 multiply to execute in one 200 nsec microcycle.

The processor has random access to the image memories for efficient execution of small area image processing as well as graphics image generation.

4. HARDWARE TRANSFORMATION UNIT

The Multiplier Accumulator Module is primarily a three dimension point transformation unit with perspective division. A 3-D transformation without division executes in less than 3 microseconds; with division, it executes in less than 5 microseconds.

The MA 1024/D is a microprogrammable device in itself. Ikonas provides routines for 2-D and 3-D point transformations, and vector dot and cross product calculations. The user can code the MA1024/D to execute spline evaluation algorithms.

5. ARCHITECTURE DESIGNED FOR 3-D SMOOTH SHADED OBJECT DISPLAY

The architecture of the RDS-3000 is specifically designed to allow efficient execution of the computations required to display smooth shaded three dimensional objects.

The Matrix Multiplier and the Processor can be executing different portions of the total display algorithm in parallel. The MA 1024/D does not use the IKONAS BUS to access the stored data base. Consequently, its operation does not reduce the performance of the processor. The Processor accesses microcode through an auxiliary BUS, again minimizing use of the IKONAS BUS.

The Image Memories in the IKONAS system have a "display-then-erase" mode which allows the memories to be cleared as they are displayed. This feature is useful in Double-Buffered or "Ping-Pong" displays. Additionally, each memory has both a write and erase mask which can enable or disable "write to" or "display-then-erase" of any bit plane.

Double-Buffering in the system can be accomplished in two ways:

1. Use of the Cross Bar Switch (or Channel Cross Bar of the LUVO module) to route different bit planes of stored display to the look-up table inputs.

2. Use of different windows in stored memory, e.g. in the DR256 Ping-Pong between two of the four 1024 x 1024 quadrants.

In each case, the switch from one displayed area to another can occur during retrace and be unnoticed by the viewer.

6. EXPANDABILITY

The IKONAS system may be field upgraded with the following optional modules.

1. Multiperipheral Controller (MPC) and Peripheral Control Panel (PCP)

   Motorola 68000 based module which allows interactive peripherals to be interfaced to the IKONAS bus system directly. Module may be upgraded to include 256K bytes of RAM. The MPC can be used as a stand-alone host by the addition of the UNIX operating system which will be available from IKONAS in third quarter 1982. The MPC ports may be expanded to include analog and TTL parallel inputs by adding the Peripheral Control Panel (PCP) to the System.

2. Video Input (VI8, VI24)

   The Video Input module or "Frame Grabber" can be supplied with either one or three 8 bit channels, allowing real time input of standard television signals. The digitizer can optionally be used with an externally supplied sample clock to allow digitization of data at varying rates up to 15MHz.

3. Hardware Character Generator (CGM)

   The CGM allows the generation of characters and user defined symbols (up to 32 x 32 pixels) to be generated and written into image memory by operations executing in parallel with the Bit Slicer processor and Multiplier-Accumulator. The CGM is recommended only for the most demanding "real-time" simulation environments.

4. Video Rate Processing Module (VPM)

   The VPM adds full frame image processing capability to the RDS-3000. Addition, subtraction, multiplication and logical operations execute in 1/30 second. For more complex algorithms, one frame time per multiple cycle is required. Inclusion of the VPM module allows efficient execution of standard full frame image processing such as image additional and subtraction, image averaging, filtering and

convolutions. The VPM will be available third quarter 1982.

5. Cross Bar Switch (XBS-34)

The XBS-34 allows the inputs to the Color Look-Up tables and the inputs to the overlay look-up to be programmatically assigned from any of the stored bit planes. This module allows any stored bit plane to be mapped to any look-up table or overlay channel input and is used in display of Double-Buffered operations, (Ping-Pong) Pseudo Color Images of more than 8 and less than 24 bits/pixel, and to allow use of an overlay plane or planes in systems with less than 32 bits/pixel.

"PING-PONG" OPERATION

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1.3 "PING-PONG" OPERATION

1.3.1 INTRODUCTION

To achieve dynamic graphics in a raster display system it is often advantageous to double buffer the display memory. "Ping-Pong" operation consists of displaying one buffer memory while the graphics processor is creating a picture in the other buffer memory. The usage of the two buffers swaps at some multiple of the video frame rate, so that no picture creation process is ever displayed to the viewer.

1.3.2 PICTURE CREATION

The new picture may be created by
(1) modification of existing picture
(2) complete picture generation

1.3.2.1 MODIFICATION

In the first instance a vector may be erased (by drawing with background shade) and then redrawn in a new position. This process takes two vector lists (new and old) and about twice the time recreation does. It is useful, however, when only a few vectors will change from frame to frame.

1.3.2.2 GENERATION

The second method is most useful when almost all vectors within a picture change from frame to frame. The IKONAS Frame Buffer Controller (FBC) has a "display-then-erase" mode to simplify picture recreation. As a group of pixels is displayed on the screen is simultaneously cleared to zero (erased) in the image memory. At the end of a display frame a clear display buffer is available to the graphics processor for generation of the new scene.

1.3.3 CONTROLLING PING-PONG OPERATION

A mechanism must be provided for ensuring that picture creation and display don't intermix. There are two methods available for two different display memory configurations: (1) with the memory configured as 2N x M pixels and only N x M pixels displayed at one time (2) with the memory configured a 22 bits/ pixel with only Z bits displayed at one time.

1.3.3.1 2N X M

For the first configuration, the window control register on the FBC can be used to select the displayed portion of memory. Only that portion displayed will be erased if the "display-then-erase" mode is selected. This scheme may be extended to triple buffering, etc. with ease. The picture creation routines must have the appropriate offset passed to them. This may be awkward depending on the software involved.

1.3.3.2 2Z

With the second memory configuration, an XBS24 crossbar switch or color map or special hardwired selector of some sort must be used to select which bits will be displayed. In order to selectively erase only certain bits of pixel, two pixel write mask applicable to all operations. Optionally, a dual mask may be specified where one mask is used for video functions (display-then-erase) and another mask for normal write operations. Of course, the mask values must be changed whenever the display ping-pongs but this is a small overhead. This method of operation allows some dynamic and some static bit planes within an image for maximum flexibility. The display generation software does not need to account for an offset as in the first case. Extension to triple buffering etc., is straightforward.

DUAL FRAME BUFFER OPERATION

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1.5 DUAL FRAME BUFFER OPERATION

1.5.1 INTRODUCTON

Some IKONAS RDS3000 Display Systems may be modified to have two complete frame buffer systems installed. Each subsystem comprises a frame buffer controller (FBC), image memories (DR64 or DR256), optional crossbar switch (XBS34), and look-up output (LUV024 or LUV030). Each of the subsystems can operate at an independent scan rate and format. For example one display can run 525 line 30Hz video while the other runs 1119 line 25Hz.

This document covers the physical arrangement, address assignment, and performance considerations of the dual frame buffer configuration.

1.5.2 PHYSICAL ARRANGEMENT

Because certain signals (like Horizontal Sync) are carried on the IKONAS RDS3000 backplane, the two frame buffer subsystems must be physically separated. This is accomplished at IKONAS by cutting the applicable sgnal traces. In a one chassis system this is done on the PC backplane, reserving 6 card slots for Frame Buffer 1 and 6 for 2. In a two chassis system, special connector cables are used so that one chassis, 12 slots, is reserved for one Frame Buffer and 12 slots for the other.

The physical separation is made so that only video operation is affected. All interfaces and processing devices still have access to both Frame Buffers over the IKONAS BUS.

1.5.3 ADDRESS ASSIGNMENT

The following table gives Address Assignments and bus priority level assignments for the dual subsystems. In cases where two complete frame buffers are not installed (e.g. one FBC, one DR64, and two LUVO24) this addressing scheme will also be followed. In the table only base addresses are given. The standard 14 bit $ 10 bit IKONAS Address convention is used. Each system is shipped with a configuration sheet giving all module addresses.

MODULE	FB 1 ADDRESS	FB 1 PRIORITY	FB 2 ADDRESS	FB 2 PRIORITY
FBC	30000$0	7	310000$0	5
XBS34	30200$0		30204$0	
LUVO24(30)	20300$0		20304$0	
DR64(LORES)	0$0		2000$0	
DR64(HIRES)	0$0		2000$0	
DR64(WORD)	1000$0		1300$0	
IF/IK(OPTIONAL)		4		2

1.5.4 PERFORMANCE CONSIDERATIONS

In order to accomodate the completely independent scan rates of the two frame buffer controllers, the IKONAS bus may be heavily used, signifficantly affecting access by host computers, or IKONAS BPS32 graphics processor. Several general cases are listed below with affect on memory availability.

FB 1	FB 2	Memory Cycles Available
512x512, 30Hz	off	75% (100 nsec/pixel)
512x512, 60Hz	off	45% (40nsec/pixel)
1024x1024, 30Hz	off	71% (22nsec/pixel)
512x512, 30Hz	512x512, 60Hz	32%
512x512, 60Hz	512x512, 60Hz	16%
1024x1024, 30Hz	512x512, 30Hz	59%
1024x1024, 30Hz	512x512, 50Hz	30%
1024x1024, 30Hz	1024x1024, 30Hz	57%

1.5.5 SUMMARY

The IKONAS RDS3000 can be configured with two completely independent frame buffer subsystems. This document has outlined physical arrangement, address assignment, and performance considerations for this unique capability. Contact Ikonas for additional information.